Japanese Journal of Applied Physics
Vol. 45, No. 8A, 2006, pp. 6177–6181

Simulation of Proposed Confined-Chalcogenide Phase-Change Random Access Memory for Low Reset Current by Finite Element Modelling

You YIN*, Hayato SONE and Sumio HOSAKA

Department of Nano-Material Systems, Graduate School of Engineering, Gunma University, 1-5-1 Tenjin, Kiryu, Gunma 376-8515, Japan

(Received March 23, 2006; accepted May 16, 2006; published online August 4, 2006)

A confined-chalcogenide (CC) cell structure for reducing the reset current of phase-change random access memory (PRAM) is proposed in this investigation. Both single normal-bottom-contact (NBC) (for reference) and proposed CC PRAM cells are simulated by two-dimensional finite element modelling. The simulated amorphous region of the NBC cell after reset operation is generally a semiellipse, which agrees very well with the reported experimental results. The CC cell has a rectangular amorphous region after reset operation. The reset operation current of the CC cell is much lower than that of the NBC cell. The CC cell structure needs a low reset current and a low power consumption and has a simple configuration.
[DOI: 10.1143/JJAP.45.6177]

KEYWORDS: PRAM, normal-bottom-contact (NBC) cell, confined-chalcogenide (CC) cell, low reset current, finite element modelling

1. Introduction

Phase-change random access memory (PRAM) is based on the reversible structural switching between the amorphous and crystalline states of chalcogenide alloys, which is induced by Joule heating due to current flow. PRAM exhibits many merits such as nonvolatile operation, high speed, low cost, excellent endurance to cycling, great scalability, superior radiation tolerance and good compatibility with silicon fabrication processes that, nowadays, it is widely taken as the best candidate for next-generation nonvolatile memories.[1–7)]

Recently, the high reset currents of PRAM with a technological node of 180 nm, for instance, 1.2–1.5 mA, are one of the biggest obstacles for its mass production. It is desirable to reduce the operation current to a few hundreds of μA for the practical production of low-power high-density memories.[8,9)] One of most important solutions to reducing the reset current is to optimize the structure of the PRAM cell. Ha *et al.* reported an edge contact PRAM cell and Pellizzer *et al.* proposed a μ-trench architecture to reduce reset current.[10,11)] However, the fabrication of these memory cells is much more complicated and the area of these cells is larger than that of the corresponding normal-bottom-contact (NBC) cell. In this paper, a confined-chalcogenide (CC) cell structure is proposed and analyzed thermally and electrically by two-dimensional finite element modelling. This cell has a very simple architecture and could be fabricated very easily. Energy generated by Joule heating could be more efficiently used to melt a smaller programming volume for the CC cell than for the NBC cell; thus, reset current might be remarkably reduced to a few hundreds of μA.

Kang *et al.* reported a one-dimensional heat conduction model for an electrical PRAM device with an $8F^2$ memory cell (feature size $F = 0.15\,\mu\text{m}$).[9)] To solve the impossible reset operation at a current of 2 mA when only TiN is used as a resistive heater, amorphous carbon of 5 nm thickness was chosen to be an additional heating layer in their simulation. However, the chalcogenide $Ge_2Sb_2Te_5$ (GST) was identified to have two crystalline structures, i.e., metastable face-centered cubic (FCC) and stable hexagonal structures, and in fast phase-change operation the polycrystalline GST always has an FCC crystal structure.[4)] The resistivity of crystalline GST in their simulation was taken to be $4.16 \times 10^{-6}\,\Omega\,\text{m}$, which is too low for FCC polycrystalline GST. It is believed that the simulation by Kang *et al.* adopted such a low resistivity that, unbelievably, the reset operation is impossible even at a very high current of 2 mA. Actually, FCC polycrystalline GST has a relatively high resistivity of approximately $10^{-4}\,\Omega\,\text{m}$ based on experimental results by both our group and other research groups.[6,12–14)] By our correct setting of this resistivity, the reset operation is feasible at a current of 1.2 mA as simulated in this study, which is very close to the reported experimental reset current.

Thus, in this study, we investigate our proposed CC cell structure by finite element modelling with a reference NBC cell structure based on the correct setting of the resistivity of polycrystalline GST, which is one of the most important parameters for the simulation of PRAM.

2. Principle and Modelling of PRAM

2.1 Principle of PRAM

As shown in Fig. 1, by applying a high and short electrical pulse to a PRAM cell, a programming volume of a chalcogenide alloy is heated to a temperature above the melting point (T_m) of the alloy and then the formerly melted part is quenched below a crystallization temperature (T_c) so

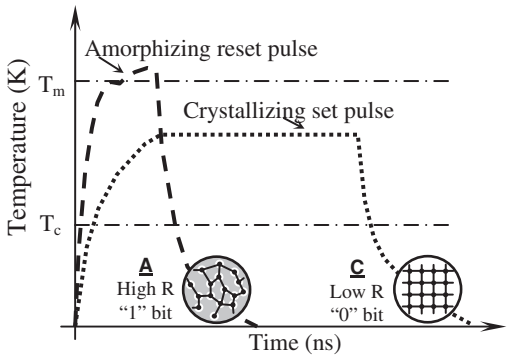

Fig. 1. Schematic diagram of phase change in PRAM cell indicating amorphizing reset and crystallizing set operations.

*E-mail address: yinyou@el.gunma-u.ac.jp

rapidly that crystallization could be sufficiently prevented. The PRAM cell then enters a highly resistive amorphous state (reset state), which could be used as logic "1" for the binary storage. This amorphizing reset operation is schematically shown as a slashed curve in Fig. 1. On the other hand, in the crystallizing set operation as a dotted curve in Fig. 1, when a low and long electrical pulse is applied to heat the chalcogenide alloy to a temperature between T_m and T_c, the programmable volume of the chalcogenide alloy layer would crystallize, and, thus, a poorly resistive crystalline state (namely, set state as logic "0") could be written into the cell.[3)]

2.2 *Finite element modelling of PRAM*

The mathematical model for heat transfer by conduction is the heat equation

$$\rho C \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = Q, \tag{1}$$

where ρ is the density, T is the temperature, C is the heat capacity, k is the thermal conductivity, t is the time and Q is the heat flux.[15)]

The heat generated by Joule heating Q is given by

$$Q = \frac{1}{\sigma} |J|^2 = \sigma |\nabla V|^2, \tag{2}$$

where σ is the electric conductivity, J is the electric current density and V is the electric potential.

Equation (1) is solved by finite element analysis in this study. The NBC and GST-CC PRAM cells are shown in Figs. 2(a) and 2(b), respectively. The NBC PRAM cell is assumed to have a Si substrate/W plug/TiN resistive heater/GST/TiN contact/W-layered structure, and the thicknesses of all the layers from the W plug are 0.5, 0.05, 0.1, 0.05, and 0.5 μm. The TiN contact and W layers are a diffusion barrier and a metal plug material, respectively.[9)] The coordinates are shown in Fig. 2, in which the x-axis is along the Si top surface and the y-axis is along the middle of each memory cell. The CC memory cell has the same GST chalcogenide area of 0.0225 μm^2 as that of the TiN resistive heater and W plug, which is smaller than that of the NBC cell. Thus, we call such a cell as a confined-chalcogenide structure. The meshed finite element modellings of the two structures are shown in Figs. 2(a) and 2(b). Refine meshes were applied to important regions of the resistive heater TiN as well as to GST chalcogenide layers for a more precise simulation of the temperature distribution in the cells.

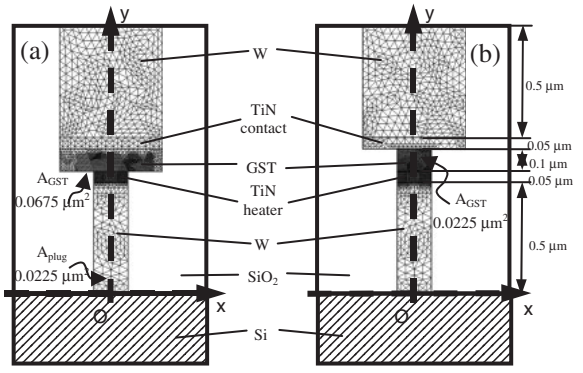

Fig. 2. Geometries and schematic cross sections of (a) NBC PRAM cell and (b) CC PRAM cell with meshed finite element models.

3. Two-Dimensional Simulation Results and Discussion

Before we describe our simulation results, some boundary conditions will be given first. The junction temperature T_J (corresponding to the bottom of meshed PRAM cell) reaches 353 K at 3.3 or 5 V operation voltage in microelectronics and the top of the W layer (corresponding to the top of meshed PRAM cell) remains at room temperature (298 K).[9)]

To simplify the simulation, the following assumption is taken into account: the temperature dependences of the thermal and electrical properties of the materials are neglected.

The required thermal and electrical properties of materials used in the simulation are given in Table I.[6,9,12–14)]

3.1 *Thermal conduction when programming*

It is very important to investigate the temperature distribution under actual device operation conditions. For instance, a constant current pulse with a width of 30 ns was actually used for reset operation.[7)] Although 0.8 mA is not a typical reset current for NBC cell, it is proved that a comparison between the temperature distributions of the two cells is very feasible at this current. Thus, in this section, a constant current pulse of 0.8 mA and 30 ns will be used for the simulation of heat transfer when programming, which is schematically shown in Fig. 6. The on-current period of the pulse is 30 ns and starts from 0 ns. After the on-current period, it enters the off-current period of the pulse.

Figures 3(a) and 3(b) illustrate the temperature distributions as well as the heat fluxes of the NBC and CC cells at the end of the on-current period (time = 30 ns), respectively. The corresponding surface temperature of the models can be determined from the gray level bar on the right side. The heat flux is shown as arrows. For each arrow, the size corresponds to the heat flux density and the direction corresponds to the heat flux direction.

The maximum temperature of the GST region of the NBC cell at a current of 0.8 mA is approximately 640 K, which is much lower than the melting temperature of GST, 905 K.

Table I. Physical properties of materials used in simulation.

Material	Melting point T_m (K)	Density ρ (kg/m^3)	Specific heat C (J/kg K)	Thermal cond. k (W/m K)	Resistivity ρ_e (Ω m)
FCC-$Ge_2Sb_2Te_5$	905	6200	202	0.46	1.0×10^{-4}
TiN Contact	3223	5240	784	22	2×10^{-7}
TiN Heater	3223	5240	784	0.44	1×10^{-5}
W	3680	19300	132	174	5.39×10^{-8}

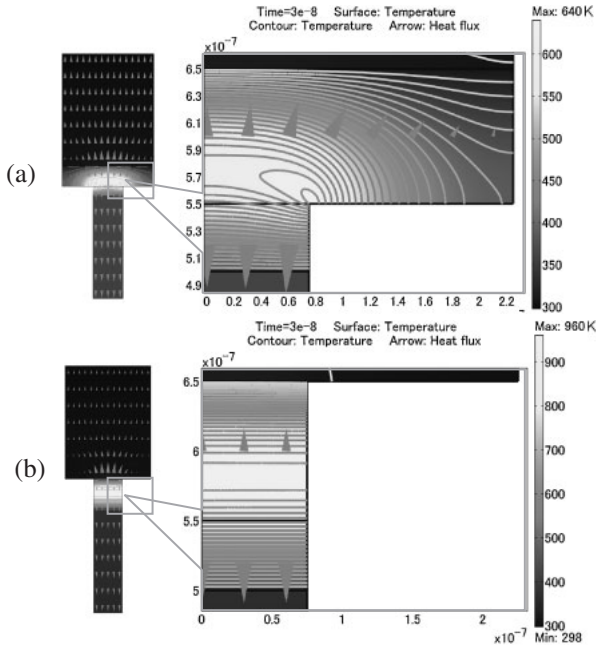

Fig. 3. Temperature distributions and heat fluxes of (a) NBC cell and (b) CC cell at the end of on-current period of pulse of 0.8 mA and 30 ns, which are schematically shown in Fig. 6. The isothermal contours of the NBC cell are very different from those of CC cell.

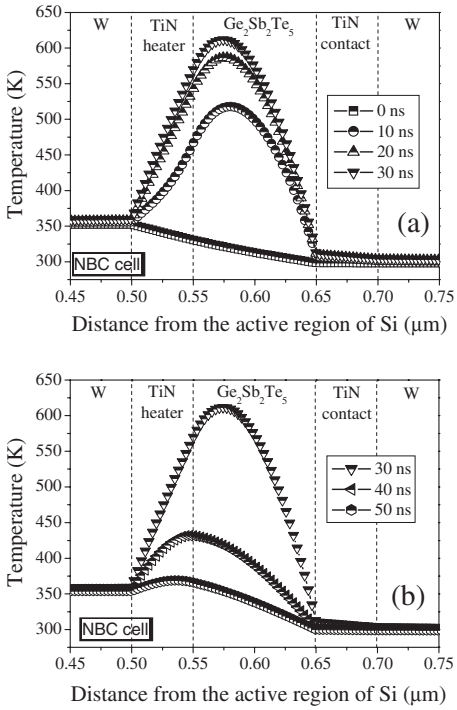

Fig. 4. Temperature profiles in (a) on-current period and (b) off-current period of NBC cell along *y*-axis in Fig. 2(a) when applying a pulse of 0.8 mA and 30 ns, which are schematically shown in Fig. 6.

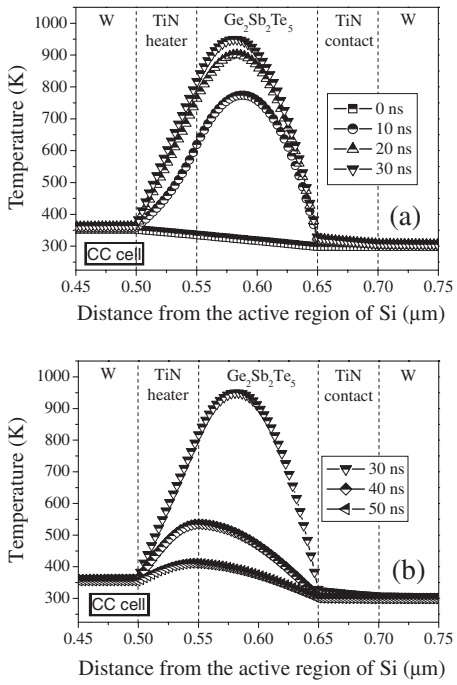

Fig. 5. Temperature profiles in (a) on-current period and (b) off-current period of CC cell along *y*-axis in Fig. 2(b) when applying a pulse of 0.8 mA and 30 ns, which are schematically shown in Fig. 6.

The high-temperature region (bright region) is likely to be programmed in that this region could reach melting temperature at first when a suitable current pulse is applied to the cell. The high-temperature bright region is located immediately on the top of the TiN resistive heater and is semi-elliptical. However, when we take a closer look at isothermal contours, the highest temperature is obviously located at the edge of the contact area between the GST layer and the resistive TiN heater layer. As a consequence, a phase distribution in the GST layer resulting from the programming pulse might have both series and parallel phase compositions as described in ref. 16, depending on the amplitude of the programming pulse, although the series phase distribution would be more controllable on the basis of the analysis of isothermal contours. A detailed discussion on phase distribution will be published elsewhere.

On the other hand, a constant current pulse of 0.8 mA and 30 ns applied to the CC cell could lead to a maximum temperature of the GST layer of approximately 960 K, much higher than the melting point of GST. Consequently, a reset operation is possible at a current of 0.8 mA for the CC cell. The isothermal contour is composed of two parallel lines and thus the programming region of the CC cell is rectangular. Only the series phase distribution would be possible from the analysis of the isothermal contour.

Detailed temperature profiles along the *y*-axis of the NBC cell in the on- and off-current periods induced by a constant current pulse of 0.8 mA and 30 ns are shown in Figs. 4(a) and 4(b), respectively. The maximum temperature is observed in approximately one third of the GST layer from the interface between the GST and TiN heater layers in the on-current period (0–30 ns), whereas it gradually shifts to the TiN heater layer in the off-current period. This is caused by different thermal conductivities of the TiN heater ($k = 0.44\,\mathrm{W/m\,K}$) and TiN contact ($k = 22\,\mathrm{W/m\,K}$). Heat flux is faster from the GST into the above TiN contact and then to the W layer than from the GST into the underlying TiN heater and then to the W plug. Figure 5 shows the temperature profiles along the *y*-axis of the CC cell, which is similar to those of NBC cell, except that a higher temperature is obtained in the GST layer of CC cell.

Figures 6(a) and 6(b) show the temperature changes at

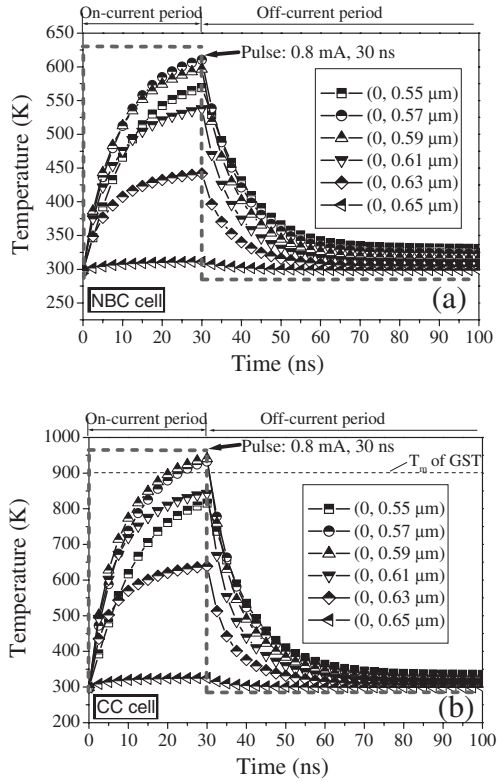

Fig. 6. Temperature change at positions in GST layer of (a) NBC cell and (b) CC cell along *y*-axis when applying a pulse of 0.8 mA and 30 ns, as schematically shown in the figures.

positions in the GST layers of the NBC and CC cells along the *y*-axis, respectively. The melting temperature of GST is drawn in Fig. 6(b) for reference. To more clearly illustrate the temperature change during on- and off-current periods, the pulse of 0.8 mA and 30 ns is schematically shown in the figures. Positions (0, 0.55 μm) and (0, 0.65 μm) are the centers of the interfaces GST/TiN heater and GST/TiN contact, respectively. At the beginning of on-current period of the pulse from 0 to 10 ns, the temperature of the GST layer due to Joule heating increases almost linearly, but the temperature increase slows down obviously between 20 and 30 ns in that the thermal balance is gradually reached. Temperature drops from the highest temperatures to approximately the crystallization temperature (for example, 473 K) within 10–15 ns after the on-current period. The quench speed is so high that the amorphization in the NBC cell as well as in the CC cell is available on the basis of our simulated results. It is also clearly seen from Fig. 6 that the maximum temperature for the CC cell is much higher than that for the NBC cell at the same current of 0.8 mA.

3.2 Reset behavior

To investigate reset behavior in detail, melted regions induced by pulses of 30 ns with different amplitudes are simulated. As is well known, the melted GST region in PRAM cell quenches below the crystallization temperature (more exactly, glass temperature) so fast that the disordered structure of GST during melting is frozen and kept even at room temperature. As a result, the melted region at the end of the on-current period (time = 30 ns) becomes the amorphous phase after the pulse application because fast

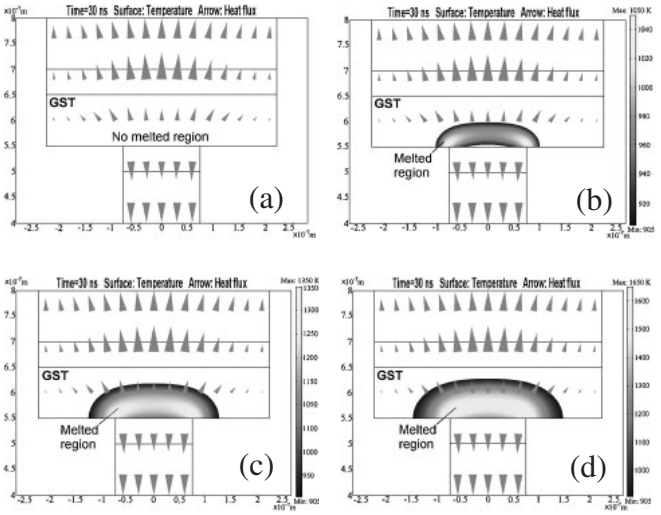

Fig. 7. Melted regions (>905 K) of NBC cell after applying pulses with increasing amplitude at 30 ns. The pulse amplitudes are (a) 1.0, (b) 1.2, (c) 1.4, and (d) 1.6 mA, respectively.

quenching is available based on our above simulated results. In other words, the melted region during the pulse application can be regarded as the amorphous phase after the pulse application.

Figures 7(a)–7(d) show the simulated melted regions of the NBC cell 30 ns after the application of a constant-current pulse with amplitudes of 1.0, 1.2, 1.4, and 1.6 mA, respectively. As shown in Fig. 7(a), the maximum temperature of the GST layer is still lower than the melting temperature, i.e., 905 K, at the end of the on-current period. In other words, reset operation is impossible at 1.0 mA in that there is no melted region in the GST layer. The region located at the bottom of the GST layer begins to melt but a small region immediately above the TiN heater still remains polycrystalline at 1.2 mA, as shown in Fig. 7(b). This could be well understood if we refer to the isothermal contour of the NBC cell in Fig. 3(a). With an increase in current pulse amplitude, the melted GST region becomes a semiellipse and grows larger as shown in Figs. 7(c) and 7(d). The semiellipse of the melted GST region agrees well with the observed amorphous region by scanning electron microscopy or transmission electron microscopy.[17)]

The melted regions of CC cell at the end of the on-current period are shown in Fig. 8. There is no melted region in the GST layer at 0.6 mA. The melted regions located at the bottom of the GST layer are rectangular and grow larger with an increase in current pulse amplitude from 0.8 mA.

The melted region at the end of on-current period could be assumed as the amorphous phase after the pulse application when we calculate device resistance after programming. As described in ref. 9, the total circuit resistance R_c range is 1000–1500 Ω. The simulated relationships between the device resistance and programming current of both the NBC and CC cells are plotted in Fig. 9, taking R_c to be 1000 Ω. The simulated reset current of the NBC cell is approximately 1.2 mA, which is in good agreement with the reported experimental results.[2,17,18)] The reset current of the CC cell is approximately 800 μA, which is about two-thirds that of the NBC cell. Thus, by adopting the proposed CC

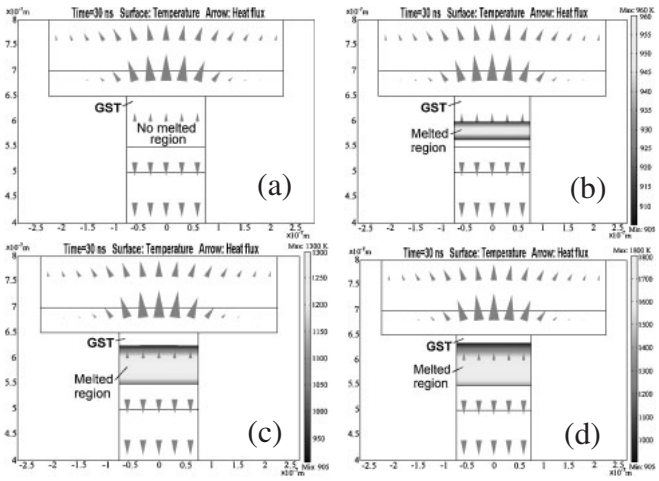

Fig. 8. Melted regions (>905 K) of CC cell after applying pulses with increasing amplitude at 30 ns. The pulse amplitudes are (a) 0.6, (b) 0.8, (c) 1.0, and (d) 1.2 mA, respectively.

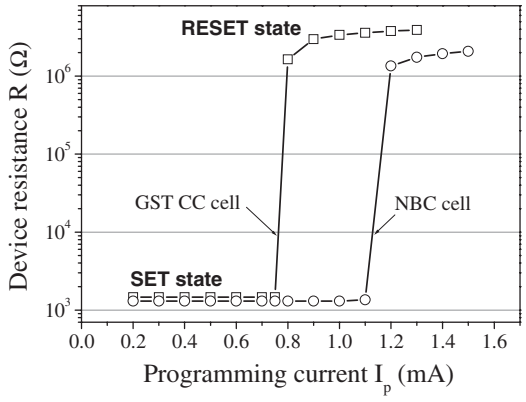

Fig. 9. Relationships between device resistance R and programming current I_p of NBC and CC cells. The GST CC cell has much lower reset current than the NBC cell.

PRAM cell, the operation current could be successfully reduced to a few hundreds of μA for low-power high-density memories. The CC cell structure has a simple configuration, a low reset current and a low power consumption so that it could be suitable for future production.

4. Conclusions

By correcting the resistivity of polycrystalline GST in PRAM, we investigated our proposed confined-chalcogenide (CC) cell structure and compared it with an NBC cell structure by two-dimensional finite element analysis. The following conclusions were drawn on the basis of the comparison of the simulated results of the NBC and CC cells.

(1) Generally, the amorphous phase region is a semiellipse in the NBC cell, whereas it is rectangular in the CC cell after the reset operation.
(2) A phase distribution in the GST layer of the NBC cell resulting from the programming pulse might have both series and parallel phase compositions, depending on the amplitude of the programming pulse.
(3) The reset of the CC cell could be operated at 800 μA for low-power high-density memories, compared with that of the conventional NBC cell.
(4) The shape of the amorphized GST region and reset current of the NBC cell are in good agreement with the reported experimental results.

Acknowledgments

This work was partially supported by the Semiconductor Technology Academic Research Center (STARC).

1) S. R. Ovshinsky: Phys. Rev. Lett. **21** (1968) 1450.
2) S. Lai and T. Lowrey: IEDM Tech. Dig., 2001, Session 36.5.
3) Y. Yin, A. Miyachi, D. Niida, H. Sone and S. Hosaka: Jpn. J. Appl. Phys. **45** (2006) 3238.
4) Y. Yin, H. Sone and S. Hosaka: Jpn. J. Appl. Phys. **44** (2005) 6208.
5) S. Hosaka, K. Miyauchi, T. Tamura, H. Sone and H. Koyanagi: Microelectron. Eng. **73–74** (2004) 736.
6) Y. Yin, A. Miyachi, D. Niida, H. Sone and S. Hosaka: 2005 IEEE Int. Conf. Electron Devices and Solid-State Circuits, Hongkong, China, 2005, p. 617.
7) Y. Yin, H. Sone and S. Hosaka: Jpn. J. Appl. Phys. **45** (2006) 4951.
8) S. Lai: IEDM Tech. Dig., 2003, p. 10.1.1.
9) D. H. Kang, D. H. Ahn, K. B. Kim, J. F. Webb and K. W. Yi: J. Appl. Phys. **94** (2003) 3536.
10) Y. H. Ha, J. H. Yi, H. Horii, J. H. Park, S. H. Joo, S. O. Park, U. Chung and J. T. Moon: Symp. VLSI Technology Dig. Tech. Pap., 2003, p. 175.
11) E. Varesi, A. Modelli, P. Besana, T. Marangon, F. Pellizzer, A. Pirovano and R. Bez: presented at EPCOS 04.
12) I. Friedrish, V. Weidenhof, W. Njoroge, P. Franz and M. Wuttig: J. Appl. Phys. **87** (2000) 4130.
13) R. Zhao, T. C. Chong, L. P. Shi, P. K. Tan, H. Meng, X. Hu, K. B. Li and A. Y. Du: Mater. Res. Soc. Symp. Proc. **803** (2004) 89.
14) T. A. Lowrey, S. J. Hudgens, W. Czubatyj, C. H. Dennison, S. A. Kostylev and G. C. Wicker: Mater. Res. Soc. Symp. Proc. **803** (2004) 101.
15) F. P. Incropera and D. P. Dewitt: *Fundamentals of Heat and Mass Transfer* (John Wiley & Sons, New York, 1996) 4th ed.
16) D. Ielmini, A. L. Lacaita, A. Pirovano, F. Pellizzer and R. Bez: IEEE Electron Device Lett. **25** (2004) 507.
17) F. Yeung, S. J. Ahn, Y. N. Hwang, C. W. Jeong, Y. J. Song, S. Y. Lee, S. H. Lee, K. C. Ryoo, J. H. Park, J. M. Shin, W. C. Jeong, Y. T. Kim, G. H. Koh, G. T. Jeong, H. S. Jeong and K. Kim: Jpn. J. Appl. Phys. **44** (2005) 2691.
18) M. Gill, T. Lowrey and J. Park: Dig. Tech. Pap. Int. Solid-State Circuits Conf., San Fransisco, CA, 2002, p. 202.